

Applicant: Arup Bhattacharyya

Docket No.: 1303.111US1

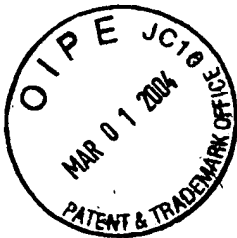
Filed: July 2, 2003

Examiner: Unknown

Serial No.: 10/612793

Due Date: N/A

Group Art Unit: 2811



Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ A Communication Concerning Related Applications (1 pg.).
- ☒ An Information Disclosure Statement (2 pgs.), Form 1449 (2 pgs.), and copies of 20 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

Customer Number 21186

By:

Atty: Marvin L. Beekman

Reg. No. 38,377

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

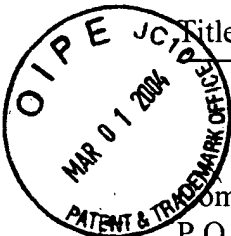
(GENERAL)

S/N 10/612793

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Arup Bhattacharyya Examiner: Unknown
Serial No.: 10/612793 Group Art Unit: 2811
Filed: July 2, 2003 Docket: 1303.111US1
Title: HIGH-PERFORMANCE ONE-TRANSISTOR MEMORY CELL



COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
10/232855	August 30, 2002	1303.072US1	GATED LATERAL THYRISTOR-BASED RANDOM ACCESS MEMORY CELL (GLTRAM)
10/232848	August 30, 2002	1303.073US1	ONE-DEVICE NON-VOLATILE RANDOM ACCESS MEMORY CELL
10/232846	August 30, 2002	1303.080US1	ONE TRANSISTOR SOI NON-VOLATILE RANDOM ACCESS MEMORY CELL
10/425483	April 29, 2003	1303.105US1	ONE TRANSISTOR SOI NON-VOLATILE RANDOM ACCESS MEMORY CELL

Respectfully submitted,

ARUP BHATTACHARYYA

By Applicant's Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6960

Date 2-25-04

By

Marvin L. Beekman

Marvin L. Beekman

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Judith Dent

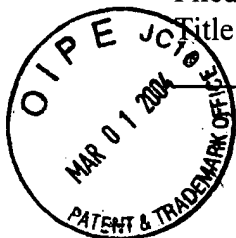
Name

Judith Dent

Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Arup Bhattacharyya	Examiner:	Unknown
Serial No.:	10/612793	Group Art Unit:	2811
Filed:	July 02, 2003	Docket:	1303.111US1
Title:	HIGH-PERFORMANCE ONE-TRANSISTOR MEMORY CELL		



INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

INFORMATION DISCLOSURE STATEMENT

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Serial No :10/612793

Dkt: 1303.111US1

Filing Date: July 02, 2003

Title: HIGH-PERFORMANCE ONE-TRANSISTOR MEMORY CELL

The present application is either a U.S. national patent application filed after June 30, 2003 or an international application that entered the national stage under 35 U.S.C. § 371 after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

ARUP BHATTACHARYYA

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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Date 2-25-04

By Marvin L. Beekman

Marvin L. Beekman

Reg. No. 38,377

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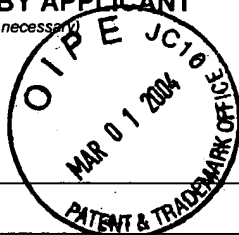
Judith Dent
Name

Judith Dent
Signature

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Complete if Known

Application Number	10/612793
Filing Date	July 2, 2003
First Named Inventor	Bhattacharyya, Arup
Group Art Unit	2811
Examiner Name	Unknown

Sheet 1 of 2

Attorney Docket No: 1303.111US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-2003/0042534	03/06/2003	Bhattacharyya, Arup, et al.	257	317	08/30/2001
	US-2003/0072126	04/17/2003	Bhattacharyya, Arup	361	311	08/30/2001
	US-2003/0089942	05/15/2003	Bhattacharyya, Arup	257	310	11/09/2001
	US-2003/0151948	08/14/2003	Bhattacharyya, Arup, et al.	365	185.18	02/12/2002
	US-2003/0160277	08/28/2003	Bhattacharyya, Arup, et al.	257	503	02/27/2003
	US-2004/0014304	01/22/2004	Bhattacharyya, Arup	438	570	07/18/2002
	US-3,918,033	11/04/1975	Case, Jerry R., et al.	365	180	11/11/1974
	US-3,964,085	06/15/1976	Kahng, Duwon, et al.	428	428	08/18/1975
	US-3,978,577	09/07/1976	Bhattacharyya, Arup, et al.	29	571	06/30/1975
	US-4,488,262	12/01/1984	Basire, Dominique, et al.	365	104	06/17/1982
	US-4,791,604	12/13/1988	Lienau, Richard M., et al.	365	9	07/23/1986
	US-4,829,482	05/09/1989	Owen	365	189.09	10/18/1985
	US-4,870,470	09/26/1989	Bass Jr., Roy S., et al.	357	23.5	10/16/1987
	US-5,043,946	08/27/1991	Yamauchi, Y., et al.	365	185.08	03/07/1990
	US-5,396,454	03/07/1995	Nowak, Edward D.	365	154	09/24/1993
	US-5,621,683	04/15/1997	Young, Nigel D.	365	185.05	12/05/1995
	US-5,627,779	05/06/1997	Odake, Yoshinori, et al.	365	185.01	07/21/1995
	US-5,801,993	09/01/1998	Choi, Woong L.	365	185.28	08/07/1997
	US-5,814,853	09/29/1998	Chen, Jian	257	315	01/22/1996
	US-5,963,476	10/05/1999	Hung, C., et al.	365	185.22	11/12/1997
	US-5,981,335	11/09/1999	Chi, Min-Hwa	438	253	11/20/1997
	US-6,104,045	08/15/2000	Forbes, Leonard, et al.	257	141	05/13/1998
	US-6,201,734	03/13/2001	Sansbury, J. D., et al.	365	185.1	09/25/1998
	US-6,243,296	06/05/2001	Sansbury, James D.	365	185.18	06/22/1999
	US-6,294,427	09/25/2001	Furuhata, Tomoyuki, et al.	438	257	05/02/2000
	US-6,462,359	10/08/2002	Nemati, Farid, et al.	257	107	03/22/2001
	US-6,545,297	04/08/2003	Noble, Wendell P., et al.	257	124	05/13/1998
	US-6,574,143	06/03/2003	Nakazato, Kazuo	365	185.18	12/08/2000
	US-6,653,174	11/25/2003	Cho, Hyun-Jin, et al.	438	133	12/17/2001
	US-6,653,175	11/25/2003	Nemati, Farid, et al.	438	133	08/28/2002

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
	JP-61-166078	07/26/1986	Ariga, R.	H01L	29/78	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	10/612793
Filing Date	July 2, 2003
First Named Inventor	Bhattacharyya, Arup
Group Art Unit	2811
Examiner Name	Unknown

Sheet 2 of 2

Attorney Docket No: 1303.111US1

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		BAUER, F, et al., "Design aspects of MOS controlled thyristor elements", <u>International Electron Devices Meeting 1989. Technical Digest</u> , (1989), 297-300	
		BHATTACHARYYA, A., "Physical & Electrical Characteristics of LPCVD Silicon Rich Nitride", <u>ECS Technical Digest, J. Electrochem. Soc.</u> , 131(11), 691 RDP, New Orleans, (1984), 469C	
		CARTER, R J., "Electrical Characterization of High-k Materials Prepared By Atomic Layer CVD", <u>IWGI</u> , (2001), 94-99	
		CHANG, H R., et al., "MOS trench gate field-controlled thyristor", <u>Technical Digest - International Electron Devices Meeting</u> , (1989), 293-296	
		CHOI, J D., et al., "A0.15 um NAND Flash Technology with .11 um ² cell Size for 1 Gbit Flash Memory", <u>IEDM Technical Digest</u> , (2000), 767-770	
		FROHMAN-BENTCHKOWSKY, D., "An integrated metal-nitride-oxide-silicon (MNOS) memory", <u>Proceedings of the IEEE</u> , 57(6), (June 1969), 1190-1192	
		HAN, KWANGSEOK, "Characteristics of P-Channel Si Nano-Crystal Memory", <u>IEDM Technical Digest, International Electron Devices Meeting</u> , (December 10-13, 2000), 309-312	
		JAGAR, S., "Single grain thin-film-transistor (TFT) with SOI CMOS performance formed by metal-induced-lateral-crystallization", <u>International Electron Devices Meeting 1999. Technical Digest</u> , (1999), 293-6	
		KUMAR, M. J., "Lateral Schottky Rectifiers for Power Integrated Circuits", <u>International Workshop on the Physics of Semiconductor Devices</u> , 11th, 4746, Allied Publishers Ltd., New Delhi, India, (2002), 414-421	
		LAI, S K., et al., "Comparison and trends in Today's dominant E2 Technologies", <u>IEDM Technical Digest</u> , (1986), 580-583	
		NEMATI, F, et al., "A novel high density, low voltage SRAM cell with a vertical NDR device", <u>1998 Symposium on VLSI Technology Digest of Technical Papers</u> , (1998), 66-7	
		NEMATI, F, et al., "A novel thyristor-based SRAM cell (T-RAM) for high-speed, low-voltage, gigascale memories", <u>International Electron Devices Meeting 1999. Technical Digest</u> , (1999), 283-6	
		OHSAWA, T., "Memory design using one-transistor gain cell on SOI", <u>IEEE International Solid-State Circuits Conference. Digest of Technical Papers</u> , vol. 1, (2002), 152-455	
		OKHONIN, S., "A SOI capacitor-less 1T-DRAM concept", <u>2001 IEEE International SOI Conference. Proceedings, IEEE</u> , 2001, (2000), 153-4	
		SHINOHE, T, et al., "Ultra-high di/dt 2500 V MOS assisted gate-triggered thyristors (MAGTs) for high repetition excimer laser system", <u>International Electron Devices Meeting 1989. Technical Digest</u> , (1989), 301-4	
		SZE, S. M., "Table 3: Measured Schottky Barrier Heights", In: <u>Physics of Semiconductor Devices</u> , John Wiley & Sons, Inc., (1981), pg. 291	
		TIWARI, SANDIP, "Volatile and Non-Volatile Memories in Silicon with Nano-Crystal Storage", <u>Int'l Electron Devices Meeting: Technical Digest</u> , Washington, DC, (Dec. 1995), 521-524	
		VAN MEER, H., "Ultra-thin film fully-depleted SOI CMOS with raised G/S/D device architecture for sub-100 nm applications", <u>2001 IEEE International SOI Conference</u> , (2001), 45-6	
		ZHANG, H., "Atomic Layer Deposition of High Dielectric Constant Nanolaminates", <u>Journal of The Electrochemical Society</u> , 148(4), (April 2001), F63-F66	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

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